LOW SUPPLY-SENSITIVE AND WIDE TUNING-RANGE CMOS LC-TANK VOLTAGE-CONTROLLED OSCILLATOR MONOLITHIC INTEGRATED CIRCUIT

Field of Invention

The invention relates to voltage-controlled oscillator (VCO) circuits. More particularly, the invention relates to a monolithic integrated circuit (IC) for a low supply-sensitive and wide tuning-range VCO for low phase-noise and low power radio frequency (RF) applications using complementary-symmetry metal-oxide-semiconductor (CMOS) transistors and one LC-tank.

Background

Conventional CMOS-based low power and low phase-noise VCO monolithic IC topologies commonly used in RF applications are shown in Figs 1, 2 and 3. A conventional LC-tank VCO core 102 shown in Figs. 1a and 1b is directly biased using a supply voltage (VDD) 104 and a reference voltage (ground) 106 without any biasing component. In the LC-tank VCO core 102, an n-channel MOS transistor pair 116 and a p-channel MOS transistor pair 118 are connected to MOS varactor(s) 112 and inductor(s) 114 for oscillation operation. A control voltage is applied to the MOS varactor(s) 112 to tune the operational frequency of the LC-tank VCO core 102.

In Figs. 2a and 2b, a conventional LC-tank VCO core 202 is biased using VDD 204 and ground 206 through a p-channel MOS biasing transistor 208 connected between the VDD 204 and the LC-tank VCO core 202. A biasing voltage is applied to the gate terminal of the p-channel MOS biasing transistor 208 to effect control over a biasing current 209 for biasing the LC-tank VCO core 202. In the LC-tank VCO core 202, an n-channel MOS transistor pair 216 is connected across MOS varactor(s) 212 and a pair of inductors 214a and 214b connected in series, the n-channel MOS transistor

pair 216, the MOS varactor(s) 212 and the pair of inductors 214a and 214b operating together to provide oscillation. A control voltage is applied to the MOS varactor(s) 212 to tune the operational frequency of the LC-tank VCO core 202. Also, an n-channel MOS transistor pair 216 is employed in the LC-tank VCO core 202 to provide a negative transconductance element to compensate for the resistance loss inherent in the LC-tank VCO core 202.

In Figs. 3a and 3b, a conventional LC-tank VCO core 302 is biased using VDD 304 and ground 306 through an n-channel MOS biasing transistor 310 connected between the LC-tank VCO core 302 and the ground 306 to provide a biasing current 309. A biasing voltage is applied to the gate terminal of the n-channel MOS biasing transistor 310 to effect control over the biasing current 309. In the LC-tank VCO core 302, a p-channel MOS transistor pair 318 is connected across MOS varactor(s) 312 and a pair of inductors 314a and 314b connected in series, the p-channel MOS transistor pair 318, the MOS varactor(s) 312 and the pair of inductors 314a and 314b together performing oscillation operation. A control voltage is applied to the MOS varactor(s) 312 to tune the operational frequency of the LC-tank VCO core 302. Also, a p-channel MOS transistor pair 318 is employed in the LC-tank VCO core 302 to provide a negative transconductance element to compensate for the resistance loss inherent in the LC-tank VCO core 302.

Due to variations in biasing techniques for conventional VCO circuit topologies, the common limitations in these topologies include poor merit of frequency pushing, which depends on the sensitivity of LC-tank VCO cores to power supplies, and limited utilization of linear range of MOS varactor(s) enabling only limited frequency tuning range of the VCO circuits. There is therefore an apparent need for VCO circuits that provide improved frequency pushing and wider frequency tuning range.

Summary

Embodiments of the invention disclosed herein possess improved performance relating to frequency pushing while achieving performance on low phase noise and low power consumption. Additionally, a wider frequency tuning range is also obtained

while achieving low phase noise performance and low power consumption.

In accordance with a first aspect of the invention, a voltage-controlled oscillator circuit connected to supply and reference voltages for radio frequency operation is disclosed, the circuit comprising at least one inductor; at least one varactor connected in parallel with the at least one inductor; a pair of p-channel MOS transistors connected across the at least one varactor, each p-channel transistor having source, drain, and gate terminals, wherein the drain terminal of the first of the pair of p-channel MOS transistors is connected to the gate terminal of the second of the pair of p-channel MOS transistors and the drain terminal of second of the pair of MOS transistors being connected to the gate terminal of the first of the pair of MOS transistors; and biasing means for providing a biasing current to the voltage-controlled oscillator circuit, the biasing means configured according to one of a biasing n-channel transistor connected to the supply voltage and a biasing p-channel transistor connected to the reference voltage.

In accordance with a second aspect of the invention, a voltage-controlled oscillator circuit connected to supply and reference voltages for radio frequency operation is disclosed, the circuit comprising at least one inductor; at least one varactor connected in parallel with the at least one inductor; a pair of p-channel MOS transistors connected across the at least one varactor, each p-channel transistor having source, drain, and gate terminals, wherein the drain terminal of the first of the pair of p-channel MOS transistors is connected to the gate terminal of the second of the pair of p-channel MOS transistors and the drain terminal of second of the pair of MOS transistors being connected to the gate terminal of the first of the pair of MOS transistors; and biasing means for providing a biasing current to the voltage-controlled oscillator circuit, the biasing means configured according to a biasing n-channel transistor connected to the supply voltage and a biasing p-channel transistor connected to the reference voltage.

In accordance with a third aspect of the invention, a method for configuring a voltage-controlled oscillator circuit connected to supply and reference voltages for radio frequency operation, the method comprising the steps of providing at least one

inductor; connecting at least one varactor in parallel with the at least one inductor; connecting a pair of p-channel MOS transistors across the at least one varactor, each p-channel MOS transistor having source, drain, and gate terminals, wherein the drain terminal of the first of the pair of p-channel MOS transistors is connected to the gate terminal of the second of the pair of p-channel MOS transistors and the drain terminal of second of the pair of p- channel MOS transistors being connected to the gate terminal of the first of the pair of p-channel MOS transistors; and providing biasing means for providing a biasing current to the voltage-controlled oscillator circuit, the biasing means configured according to a biasing n-channel transistor connected to the supply voltage and a biasing p-channel transistor connected to the reference voltage.

Brief Description of Drawings

Embodiments of the invention are described hereinafter with reference to the drawings, in which:

Figs. 1a and 1b illustrate a conventional VCO circuit with an LC-tank VCO core;

Figs. 2a and 2b illustrate another conventional VCO circuit with an LC-tank VCO core;

Figs. 3a and 3b illustrate a further conventional VCO circuit with an LC-tank VCO core;

Figs. 4a and 4b illustrate a VCO circuit with an LC-tank VCO core according to a preferred embodiment of the invention;

Fig. 4c illustrates a VCO circuit with an LC-tank VCO core according to another embodiment of the invention;

Fig. 4d illustrates a VCO circuit with an LC-tank VCO core according to a further embodiment of the invention;

Fig. 5a in conjunction with Tables 1 and 2 illustrate simulated performance of the VCO circuit of Figs. 4a and 4b; and

Fig. 5b illustrates characteristics of a MOS varactor used in the VCO circuit of Figs. 4a, 4b, 4c and 4d.

Detailed Description

Embodiments of the invention are described with reference to Figs. 4a to 4d. The preferred embodiment is described with reference to Figs, 4a and 4b. In such an embodiment, an LC-tank VCO core is biased using two MOS transistors. In an alternate embodiment described with reference to 4c, an LC-tank VCO core is biased using a p-channel MOS transistor connected to a reference voltage such as ground. In a further alternative embodiment described with reference to 4d, an LC-tank VCO core is biased using an n-channel MOS transistor connected to a supply voltage such as VDD.

In Figs. 4a and 4b, an LC-tank VCO core 402 is biased using VDD 404 and ground 406 through an n-channel MOS biasing transistor 408 connected between the LC-tank VCO core 402 and the VDD 404 to provide a biasing current 409. A biasing voltage is applied to the gate terminal of the n-channel MOS biasing transistor 408 to effect control over the biasing current 409. The LC-tank VCO core 402 is further biased through a p-channel MOS biasing transistor 410 connected between the LC-tank VCO core 402 and the ground 404. The gate terminal of the p-channel MOS biasing transistor 410 is connected to the drain terminal of the p-channel MOS biasing transistor 410 for providing self-biasing.

In the LC-tank VCO core 402, a p-channel MOS transistor pair 418 is connected across the MOS varactor(s) 412 and a pair of inductors 414a and 414b connected in series; the p-channel MOS transistor pair 418, the MOS varactor(s) 412 and the pair of inductors 414a and 414b together performing oscillation operation.

A control voltage is applied to the MOS varactor(s) 412 to tune the operational frequency of the LC-tank VCO core 402. Also, a p-channel MOS transistor pair 418 is employed in the LC-tank VCO core 402 to provide a negative transconductance element to compensate for the resistance loss inherent in the LC-tank VCO core 402.

The source terminal of the n-channel MOS biasing transistor 408 is connected to the sources of the p-channel MOS transistor pair 418 while the source terminal of the p-channel MOS biasing transistor 410 is connected to the inter-connection between the pair of inductors 414a and 414b.

The n-channel MOS biasing transistor 408 operates in the saturation region and provides the biasing current 409 to the LC-tank 402. By using an n-channel MOS transistor in this instance, any change in the biasing current 409 with respect to any change in the VDD 404 is reduced. Thus, the n-channel MOS biasing transistor 408 offers a simple solution to suppress noise from the VDD 404 and as a result provides a low supply-sensitive VCO circuit with improved merit of frequency pushing.

Herein, frequency pushing is defined as the sensitivity of a VCO circuit to its supply voltage and can be expressed as following:

$$\frac{\left(\Delta f / f\right)}{\Delta V_{DD}} \ \% / V$$

where f is the center frequency given a power supply of V_{DD}, and Δf is the oscillation frequency variation due to ΔV_{DD} , the voltage change in the power supply V_{DD}.

Further improvement in frequency pushing can be achieved by increasing the channel length of the n-channel MOS biasing transistor 408 due to a lower channel length modulation effect in the longer channel devices.

The self-biasing p-channel MOS biasing transistor 410 is used to bias the MOS varactor(s) 412 to enhance utilization of linear range of the MOS varactor(s) 412. By connecting the gate terminal of the p-channel MOS biasing transistor 410 to the ground 406 exploits further usage of the linear range of the MOS varactor(s) 412 resulting in wide frequency tuning range of the VCO circuit. The following relationship shows how the variations in capacitance of the MOS varactor(s) 412 are related to the frequency tuning range of the VCO circuit:

$$\Delta\omega = \frac{1}{\sqrt{LC}} - \frac{1}{\sqrt{L(C \pm C_{\mathrm{var}})}} = \omega_0 \left(1 - \frac{1}{\sqrt{1 \pm \frac{C_{\mathrm{var}}}{C}}}\right)$$

$$= \omega_0 \left(1 - \frac{1}{\sqrt{1 \pm C_{\mathrm{var}} \omega_0^{\,2} L}}\right) \approx \pm \frac{1}{2} \omega_0^{\,3} L C_{\mathrm{var}}$$

where ω_0 is the center frequency, L is the total inductance in the LC-tank, C is the total capacitance in the LC-tank at the center frequency, and C_{var} is the maximum variable capacitance tuned by control voltage.

In Fig. 4c, an LC-tank VCO core 402 is biased using VDD 404 and ground 406 through a p-channel MOS biasing transistor 410 connected between the LC-tank VCO core 402 and the ground 406 to provide a biasing current 409. The gate terminal of the p-channel MOS biasing transistor 410 is connected to the drain terminal of the p-channel MOS biasing transistor 410 for providing self-biasing.

In the LC-tank VCO core 402, a p-channel MOS transistor pair 418 is connected across the MOS varactor(s) 412 and a pair of inductors 414a and 414b connected in series; the p-channel MOS transistor pair 418, the MOS varactor(s) 412 and the pair of inductors 414a and 414b together performing oscillation operation.

A control voltage is applied to the MOS varactor(s) 412 to tune the operational frequency of the LC-tank VCO core 402. Also, a p-channel MOS transistor pair 418 is employed in the LC-tank VCO core 402 to provide a negative transconductance

element to compensate for the resistance loss inherent in the LC-tank VCO core 402.

The VDD 404 is connected to the drains of the p-channel MOS transistor pair 418 while the source terminal of the p-channel MOS biasing transistor 410 is connected to the inter-connection between the pair of inductors 414a and 414b.

In Fig, 4d, an LC-tank VCO core 402 is biased using VDD 404 and ground 406 through an n-channel MOS biasing transistor 408 connected between the LC-tank VCO core 402 and the VDD 404 to provide a biasing current 409. A biasing voltage is applied to the gate terminal of the n-channel MOS biasing transistor 408 to effect control over the biasing current 409.

In the LC-tank VCO core 402, a p-channel MOS transistor pair 418 is connected across the MOS varactor(s) 412 and a pair of inductors 414a and 414b connected in series; the p-channel MOS transistor pair 418, the MOS varactor(s) 412 and the pair of inductors 414a and 414b together performing oscillation operation.

A control voltage is applied to the MOS varactor(s) 412 to tune the operational frequency of the LC-tank VCO core 402. Also, a p-channel MOS transistor pair 418 is employed in the LC-tank VCO core 402 to provide a negative transconductance element to compensate for the resistance loss inherent in the LC-tank VCO core 402.

The source terminal of the n-channel MOS biasing transistor 408 is connected to the sources of the p-channel MOS transistor pair 418 while the ground 406 is connected to the inter-connection between the pair of inductors 414a and 414b.

The VCO circuit according to the preferred embodiment is simulated using 0.35μm standard CMOS technology parameters. A typical set of simulated performance shown in Table 1 and Fig 5a indicate that: center frequency = 2.632 GHz, frequency tuning range = 624MHz, phase noise @ 100kHz offset from center frequency = -103dBc/Hz, frequency pushing = 0.25%/V and supply current = 4mA at 3V supply voltage using MOS varactors having characteristics as shown in Fig. 5b. The further

simulation results as shown in Table 2 indicate that the frequency pushing performance is improved by increasing the channel length of the n-channel MOS biasing transistor 408.

In the foregoing manner, there are described VCO circuits that provide improved frequency pushing and wider frequency tuning range. Although only a number of embodiments of the invention are disclosed, it becomes apparent to one skilled in the art in view of this disclosure that numerous changes and/or modification can be made without departing from the scope and spirit of the invention. For example, although all MOS transistors used in the foregoing embodiments are enhancement type MOS transistors, these may perform similar operation if substituted by depletion type MOS transistors. Furthermore, all MOS transistors used in the embodiments may perform similar operation if substituted by devices or circuits having the like characteristics such as JFET transistors.